IBIS Model User Guide for Z-One^{TM} Devices

Application Note

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Overview

IBIS models are behavioral circuit models typically used for simulating the detailed signal integrity of a digital I/O buffer with specific PCB / loading conditions. The models may be used with various commercially available simulators that have IBIS capabilities.

IBIS models contain current-voltage (I-V) and voltage-time (V-T) curves as well as package resistance, inductance, and capacitance information. The simulator changes state (1 or 0) according to the source waveform set by the user. As the state changes, the behavioral model for the driver (I-V and V-T curves) interacts with the circuit topology and receivers and a voltage versus time response is generated. The response is usually presented to the user as a waveform similar to an oscilloscope waveform. For more information, see [1].

The IBIS models are intended to be used to simulate the rise and fall waveforms for user-created topologies. For example, the Z-One™ system uses bidirectional, open drain driver / receivers for its SD (Sync/Data) and I2C serial communication buses. The SD bus is running at a 500 KHz pulse rate while the I2C runs at up to 400 KHz. The signal integrity of these signals can be affected by the PCB layout and the choice of pull-ups. For details regarding Power-One parts, see the data sheets at [2].

The IBIS models are intended to help the user with PCB layout signal integrity issues and aid in choosing the proper pull-up.

1. Model Details

Single-Pin Models – The ZY series Point-Of-Load modules (POLs) and ZM7100 DPM are represented by simple single-pin models that include only the SD pin. These models contain only typical data, no min/max data. This is sufficient for basic SD bus simulation.

Multi-Pin Model – The ZM7300 DPM is a complete model that includes every device pin as well as min/max data.

2. Simulation Recommendations

To simulate the SD waveform, inject a 500 kHz pulse with a 0.75 duty cycle at the device that is the master clock for the system (the DPM or the POL with the IM pin tied low). Observe the simulated SD waveform at various points along the SD line. Verify that the logic levels, rise and fall times are meeting the data sheet requirements.

Note that the receivers have hysteresis as called out in the data sheets, so the SD waveform does not have to be monotonic.

It is recommended that the user begin with realistic values for trace lengths and transmission line properties.

A pull-up resistor may be used in larger systems to improve the rise time. The pull up is tied to the 3.3 V pin of the DPM. Typically, a 2 kOhms resistor is adequate.

For the ZM7300, the I2C bus can be simulated by injecting a 400 KHz square wave on the SCL and SDA pins and again verifying that the data sheet values for rise and fall times and logic levels are met. Per the data sheet, the ZM7300 requires a typical pull-up of 2.5 kOhms on the SCL and SDA lines.

3. Avoiding Simulator Convergence Issues

Circuits with insufficient pull-up strength and/or excessively large or small trace impedance are likely to cause a simulator to have convergence issues. Following the simulation recommendation above will help eliminating this problem.

Should you have any questions, please, contact:

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4. References

[1] IBIS (I/O Buffer Information Specification) ANSI/EIA-656-A Homepage: http://www.eigroup.org/IBIS/
[2] Power-One data sheets are available at: http://www.power-one.com